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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Louis B. Hobson	Examiner: Jonathan R. Plante Art Unit: 2112
Serial No.: 10/812,147	
Filed: 03/29/04	
For: **Using Thermal Management Register to Simulate Processor Performance States**	
Date of Last Office Action: November 6, 2006	Attorney Docket No.: 200314997-1

February 6, 2007

AMENDMENT A

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Responsive to the Office Action of November 6, 2006, Applicant respectfully requests amendment of the application as follows:

CERTIFICATE OF FACSIMILE

Date of Deposit: February 6, 2007

I hereby certify that these papers are being transmitted to The Patent and Trademark Office facsimile number (571) 273-8300 on February 6, 2007.

Doreen Zabinski

Doreen Zabinski

Docket No. 200314997-1

Please amend the following paragraphs as indicated:

[0002] A processor performance state may specify a frequency and voltage at which a processor is to operate. To facilitate implementing a processor performance state, a processor may include an internal machine specific register (MSR) that can be programmed to control the frequency and voltage associated with a processor performance state. Additionally, a microprocessor may include hardware specifically allocated for an emergency response to an overheated condition. For example, an Intel® Pentium® 4 processor includes a thermal management register (TM2) that can be employed to facilitate controlling temperature. Conventionally, the TM2 register is accessed in response to a processor overheated (PROCHOT) signal being asserted on a line (e.g., PROCHOT line) available to the processor. The PROCHOT signal is typically generated by a thermal management circuit in response to detecting a thermal condition (e.g., overheated). For example, Prior Art Figure 1 illustrates an example circuit that can be employed to trigger the PROCHOT signal when a processor is overheating.

[0025] **Figure 2** illustrates an example system **200** for simulating processor performance states using a thermal management register in, and a thermal management signal available to a processor **230**. The thermal management register may be, for example, the TM2 register in a Pentium 4 microprocessor. Similarly, the thermal management signal may be a signal available on the PROCHOT line available to the Pentium 4 microprocessor. The system **200** may include a data structure **210** stored in a memory and/or data store. The data structure **210** may store the address(es) of a GPIO (General Purpose Input Output) block **220** and a set of bit patterns that may be written to the GPIO block **220** and/or the thermal management register. In one example, the data structure **210** may also store the address(es) of an ACPI status register(s) (not illustrated) from which a value related to a state established by the GPIO block **220** can be read.

[0028] The data structure **210** may store a set of bit patterns and the logic **240** may be configured to select a bit pattern from the data structure based on a request from the operating system **250**. For example, a request to enter a lower performance state may lead to a first bit pattern(s) being selected from a set of bit patterns while a request to enter a higher performance state may lead to a second bit pattern(s) being selected from the set of bit patterns. A lower performance state may be produced by causing a first signal (e.g., 5V) to be placed on the PROCHOT line and by a first bit pattern being provided to the TM2 register. A higher performance state may be produced by causing a second signal (e.g., 0V) to be placed on the PROCHOT line and by a second bit pattern being provided to the TM2 register. Changing the states may include causing the processor to lower its core to bus ratio and operating voltage. Concerning the bit patterns that may be stored, read, and/or processed by the system **200**, the bit patterns may control individual bit lines or may be used collectively as patterns. For example, eight bits represented as 0xff (hexadecimal) may be used to control establishing a high processor performance state (e.g., high voltage, high frequency) while eight bits represented as 0x00 (hexadecimal) may be used to control establishing a low processor performance state (e.g., low voltage, low frequency). Similarly, a bit pattern like 0xf0 may signal an intent to toggle a processor performance state from high to low or low to high. While eight bit patterns are described, it is to be appreciated that the bit patterns may be represented by a greater and/or lesser number of bits.

[0041] The method **500** may also include, at **530**, receiving a request to establish a processor performance state. The request may come from an operating system, an application, a user, and so on. In one example, the operating system may be Microsoft® Windows® XP. Instead of directly driving an internal processor frequency and an internal processor voltage by writing internal machine specific registers dedicated to implementing processor performance states, the method **500** may instead, at **540**, acquire a bit pattern that can be written to the GPIO block and/or the thermal management register. Since ACPI data structures and methods may virtualize a hardware environment, the method **500** may also include, at **550**, acquiring an address of the GPIO block to which the bit pattern acquired at **540** can be written. The bit pattern and the GPIO block address may be acquired from the

data store configured at **510** and **520**, for example. After acquiring the bit pattern and the GPIO block address, the method **500** may, at **560**, write the bit pattern to the GPIO block and/or the thermal management register. In one example, writing the bit pattern to the GPIO block causes a signal to be placed on a PROCHOT line into the processor. Placing the signal on the PROCHOT line can cause the processor to change its operating frequency and voltage and thus a processor performance state can be simulated.

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HEWLETT-PACKARD COMPANY
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Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200314997-1

Inventor(s): Louis B. Hobson

Application No.: 10/812,147

Filing Date: 03/29/2004

Confirmation No.: 2982

Examiner: Jonathan R. Plante

Group Art Unit: 2112

Title: USING THERMAL MANAGEMENT REGISTER TO SIMULATE PROCESSOR PERFORMANCE STATES

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [ ] New fee as calculated below
- [x] No additional fee
- [ ] Other
- [ ] Petition to extend time to respond
- [ ] Supplemental Declaration

Fee$

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	24	MINUS	24	= 0	X $50	$ 0
INDEP. CLAIMS	6	MINUS	8	= 0	X $200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $360	$ 0
EXTENSION FEE	☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

☐ A duplicate copy of this transmittal letter is enclosed.

I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300.
Date of facsimile: February 6, 2007

Typed Name: Doreen Zabinski

Signature: Doreen Zabinski

Respectfully submitted,

Louis B. Hobson

By Petar Kraguljac

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Rev 10/06e(TransAmdFax)